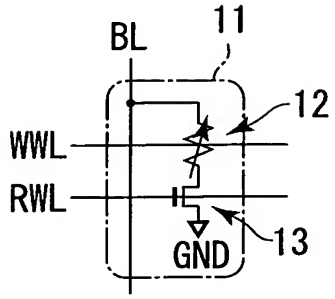


FIG. 1 (PRIOR ART)

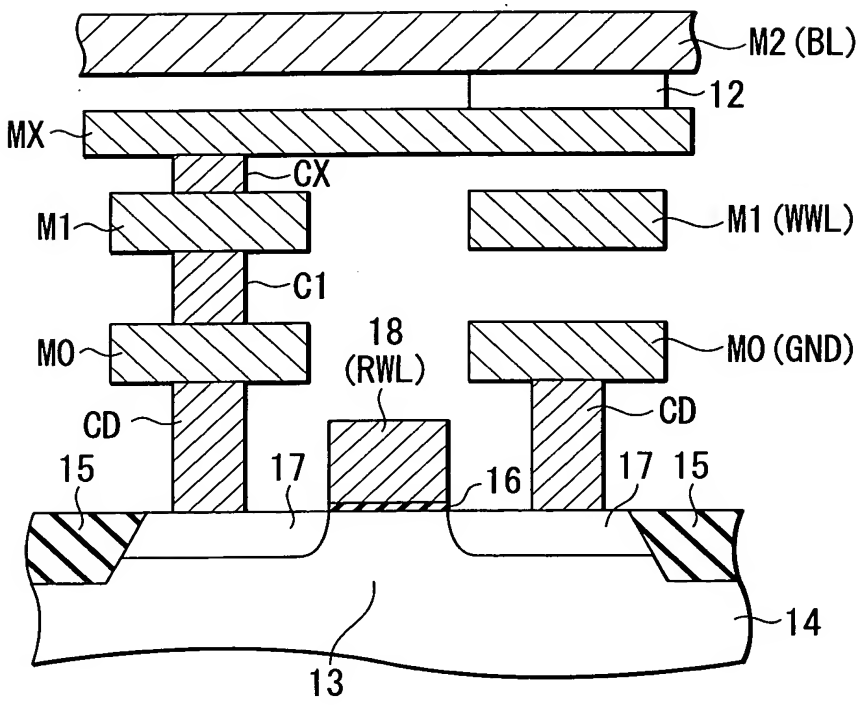


FIG. 2 (PRIOR ART)

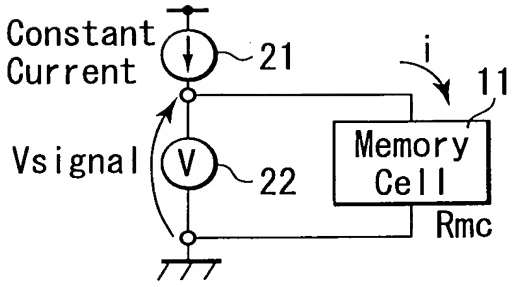


FIG. 3A (PRIOR ART)

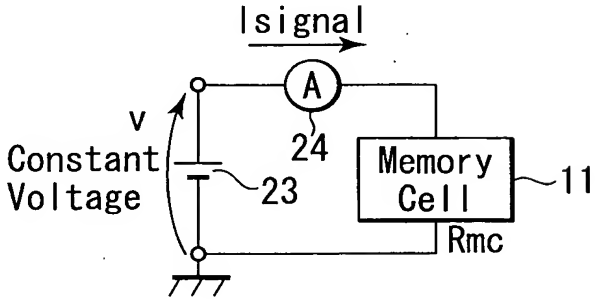


FIG. 3B (PRIOR ART)

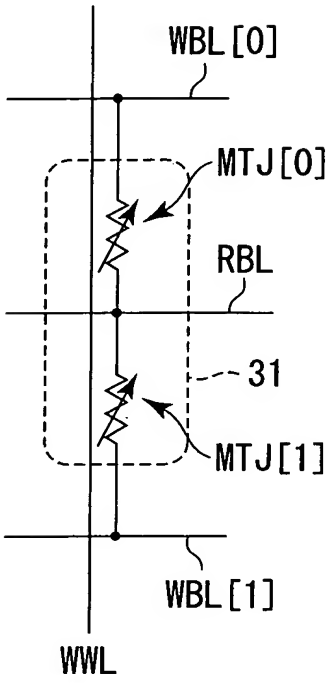


FIG. 4

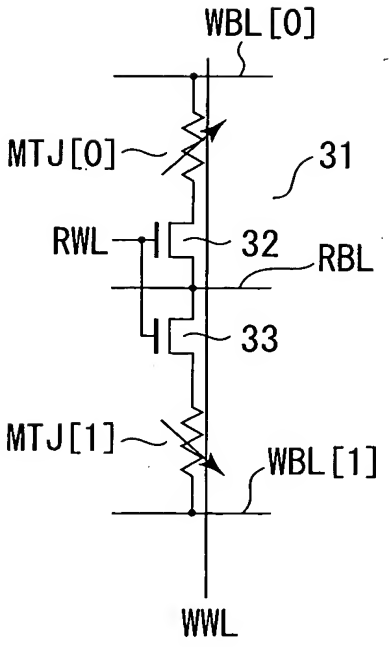


FIG. 5

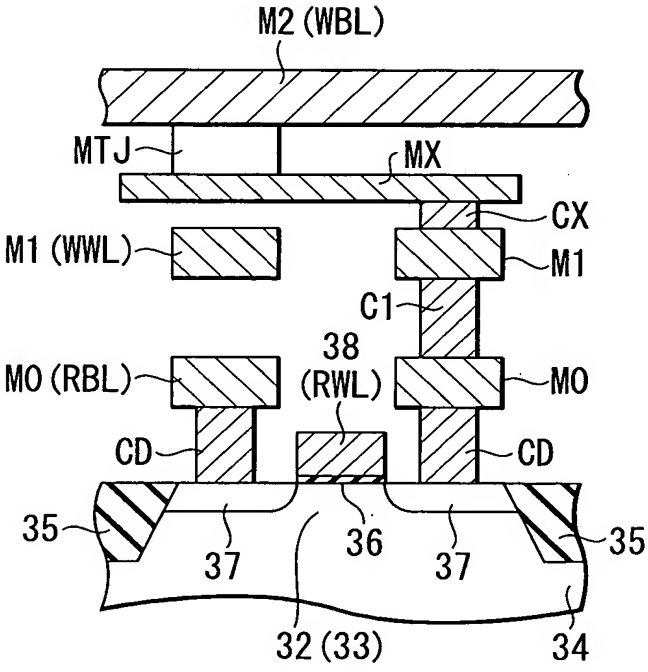


FIG. 6

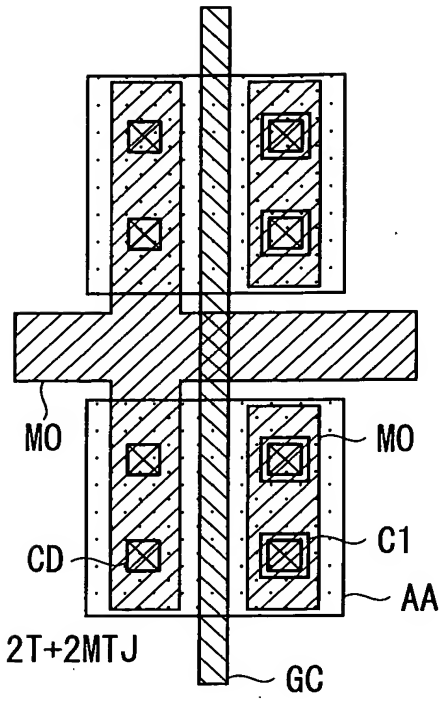


FIG. 7A

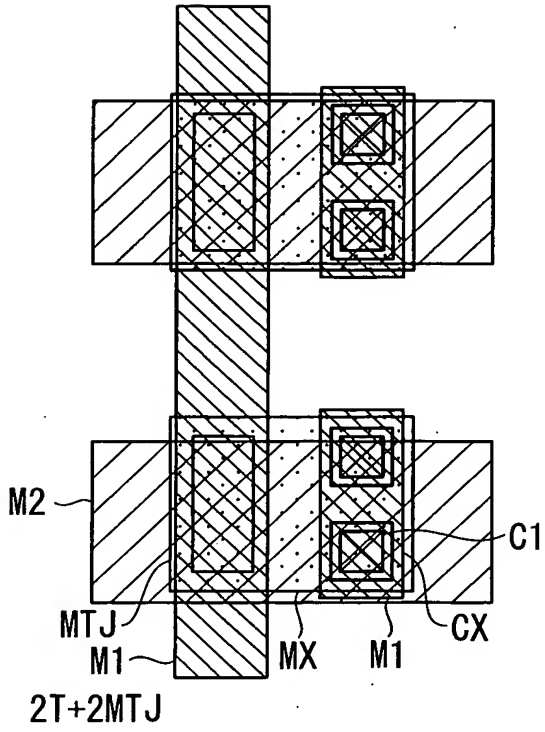


FIG. 7B

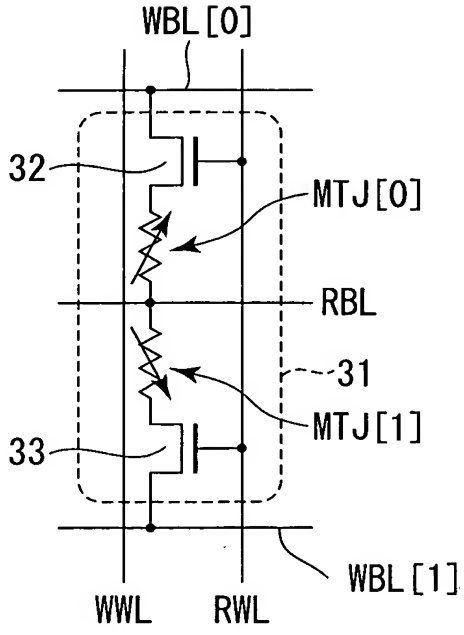


FIG. 8

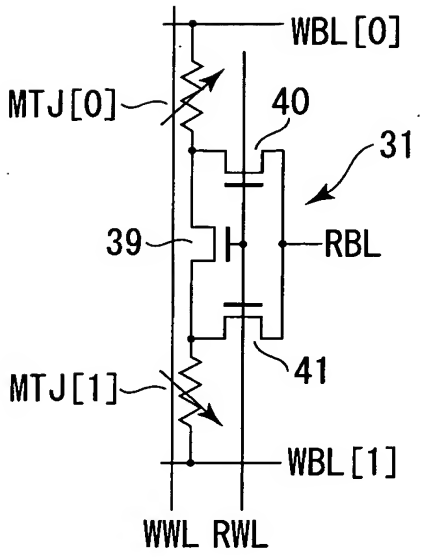


FIG. 9

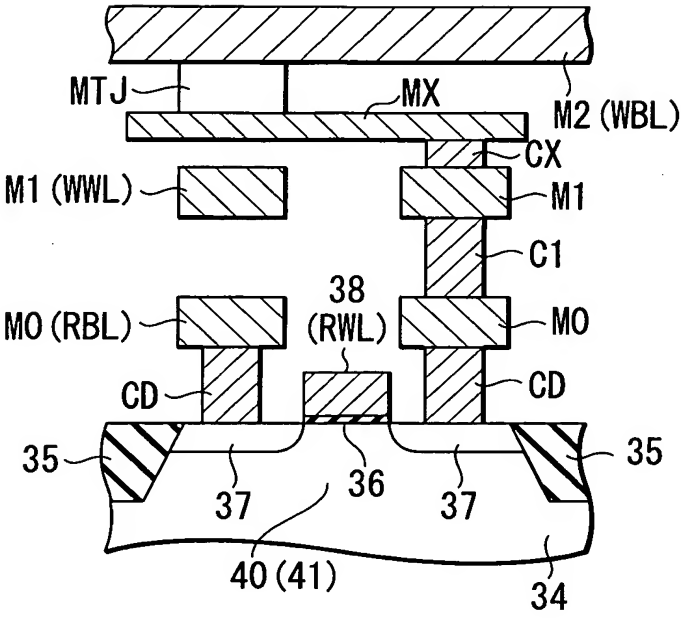


FIG. 10

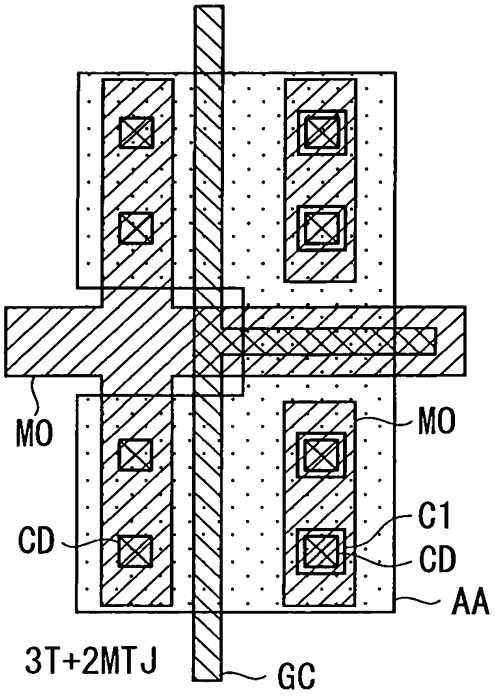


FIG. 11A

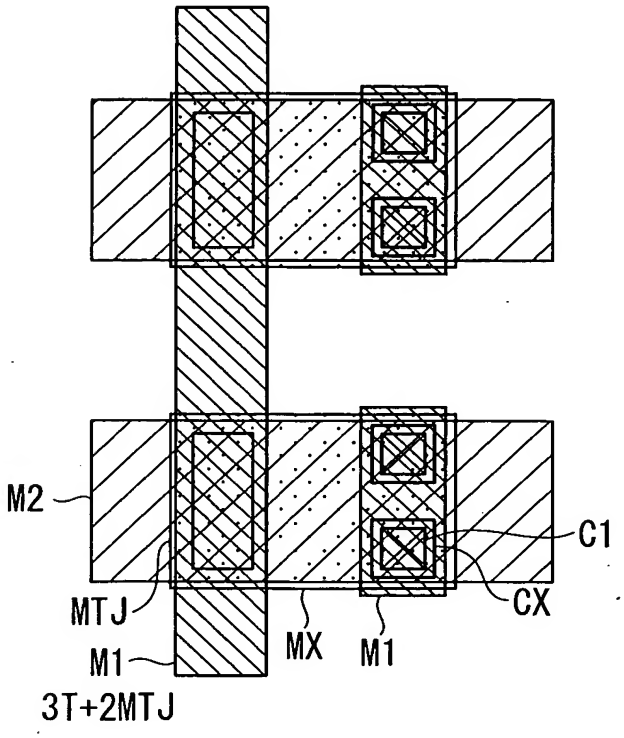


FIG. 11B

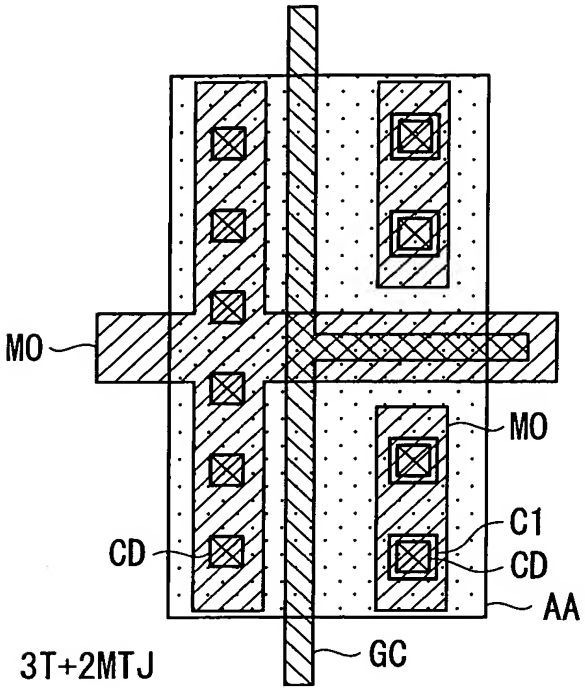


FIG. 12

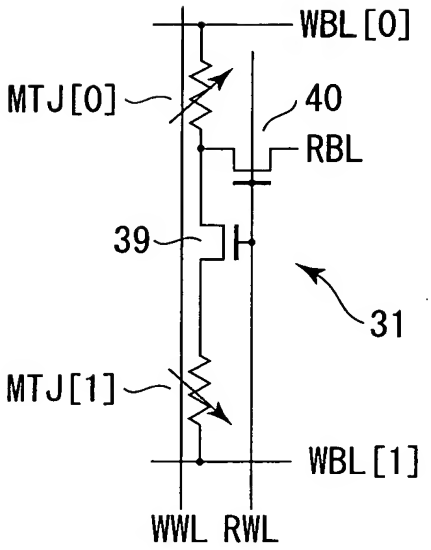


FIG. 13

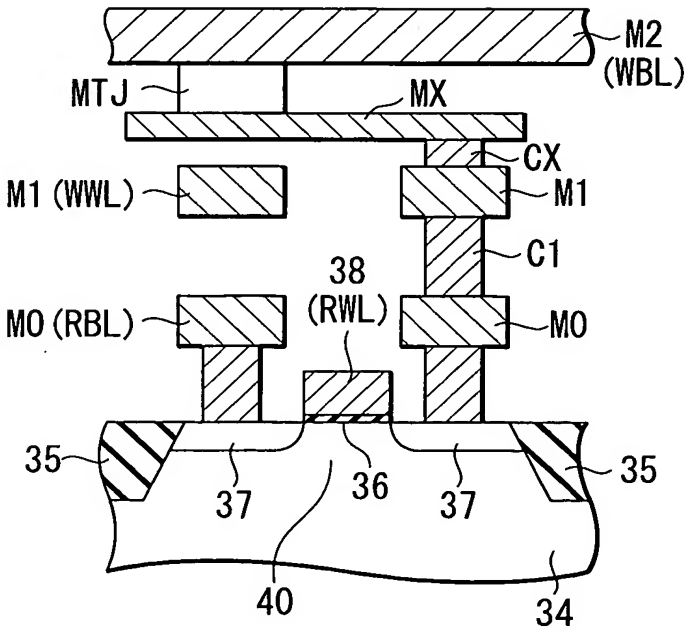


FIG. 14

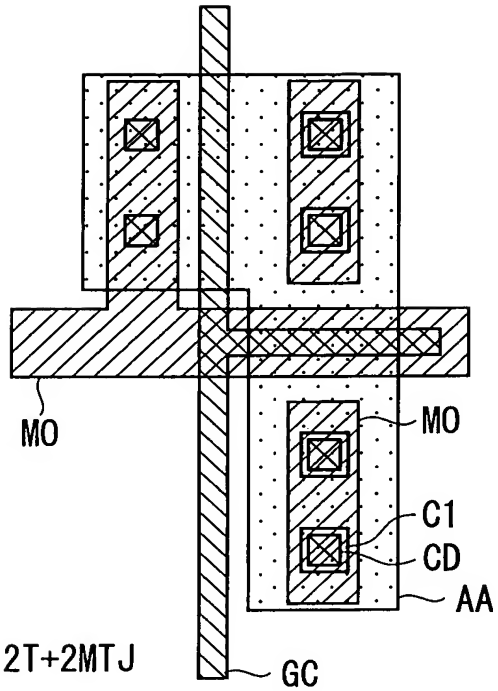


FIG. 15A

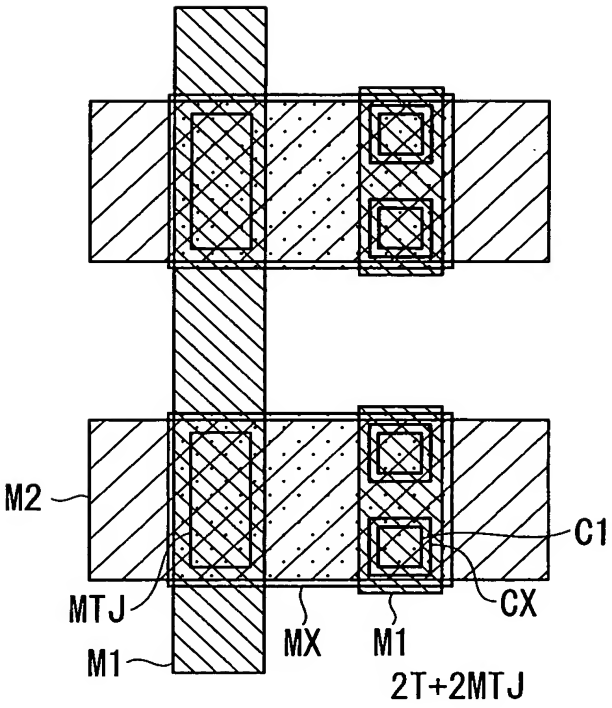


FIG. 15B

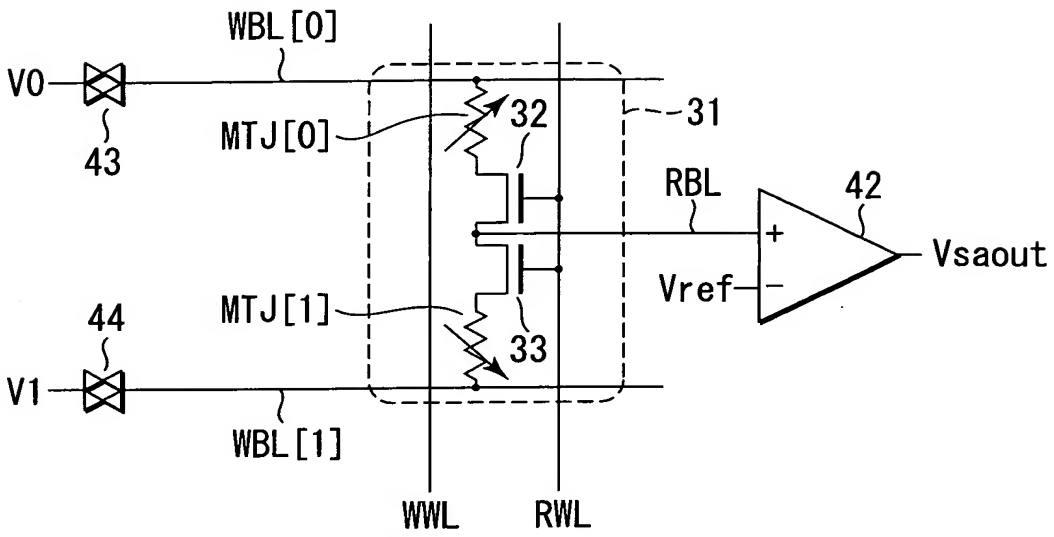

WBL[0]
V0
43
MTJ[0]
32
31
RBL
42
+
Vsaout
Vref
−
MTJ[1]
44
33
V1
WBL[1]
WWL
RWL

FIG. 16

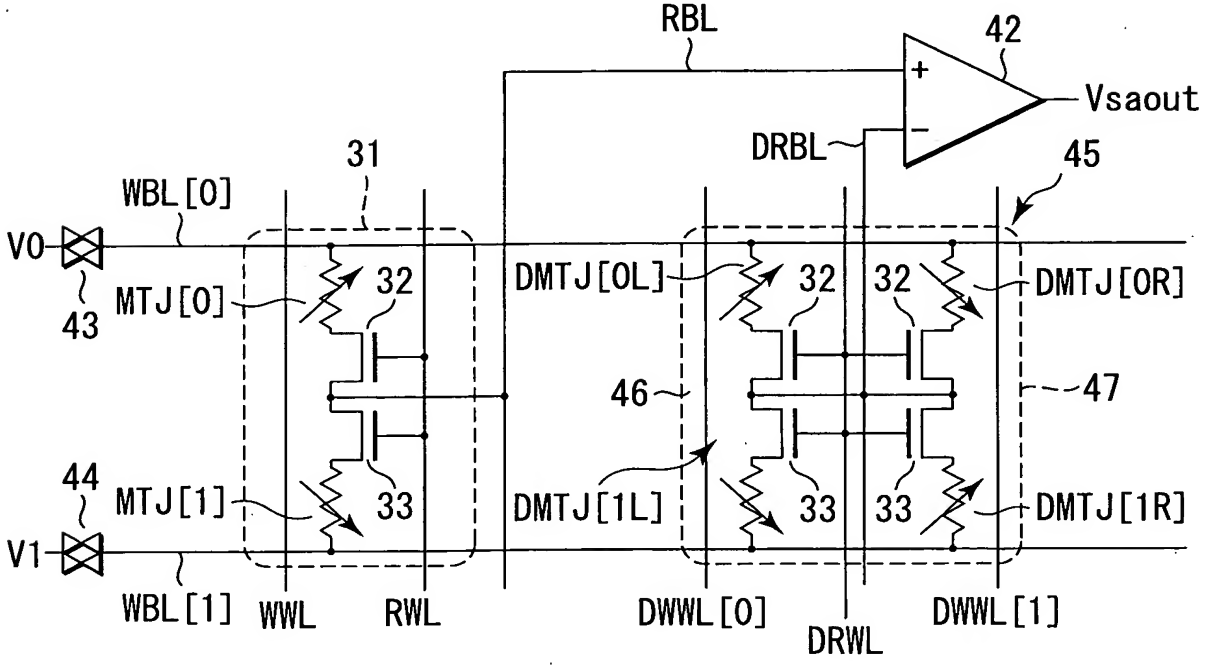

RBL
42
+
Vsaout
−
DRBL
45
31
WBL[0]
V0
43
MTJ[0]
32
DMTJ[0L]
32
32
DMTJ[0R]
46
47
44
MTJ[1]
33
DMTJ[1L]
33
33
DMTJ[1R]
V1
WBL[1]
WWL
RWL
DWWL[0]
DRWL
DWWL[1]

FIG. 17

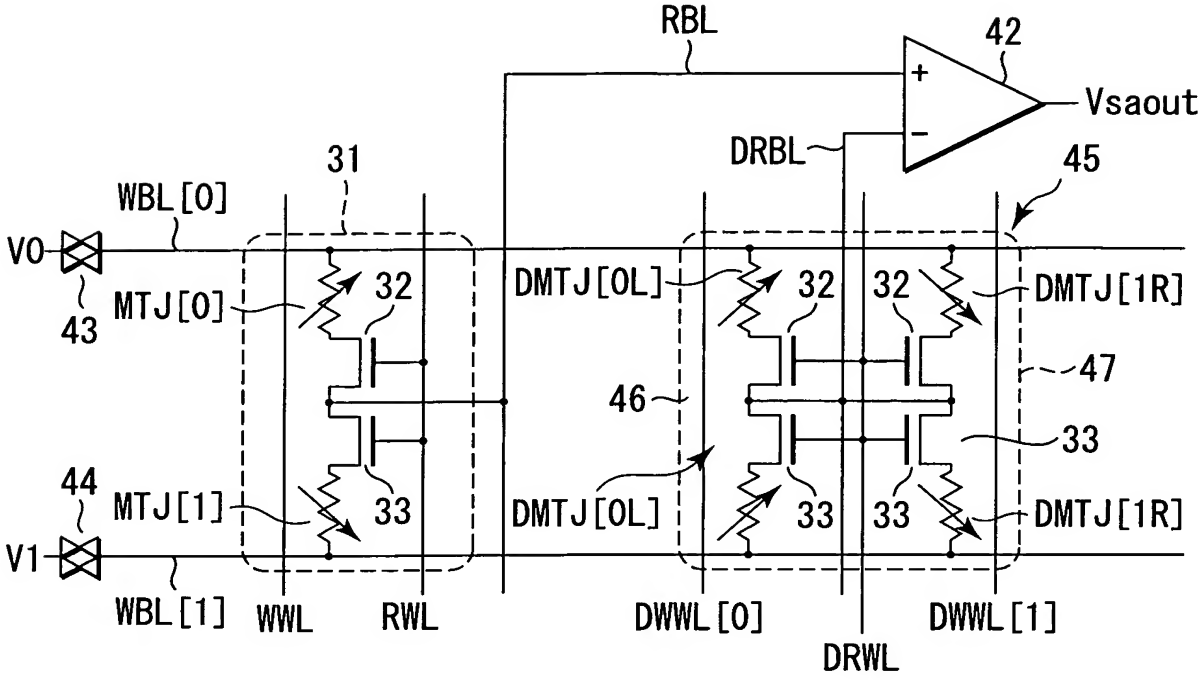

RBL
42
Vsaout
DRBL
45
31
WBL[0]
V0
43
MTJ[0]
32
DMTJ[0L]
32
32
DMTJ[1R]
47
46
33
44
MTJ[1]
33
DMTJ[0L]
33
33
DMTJ[1R]
V1
WBL[1]
WWL
RWL
DWWL[0]
DWWL[1]
DRWL

FIG. 18

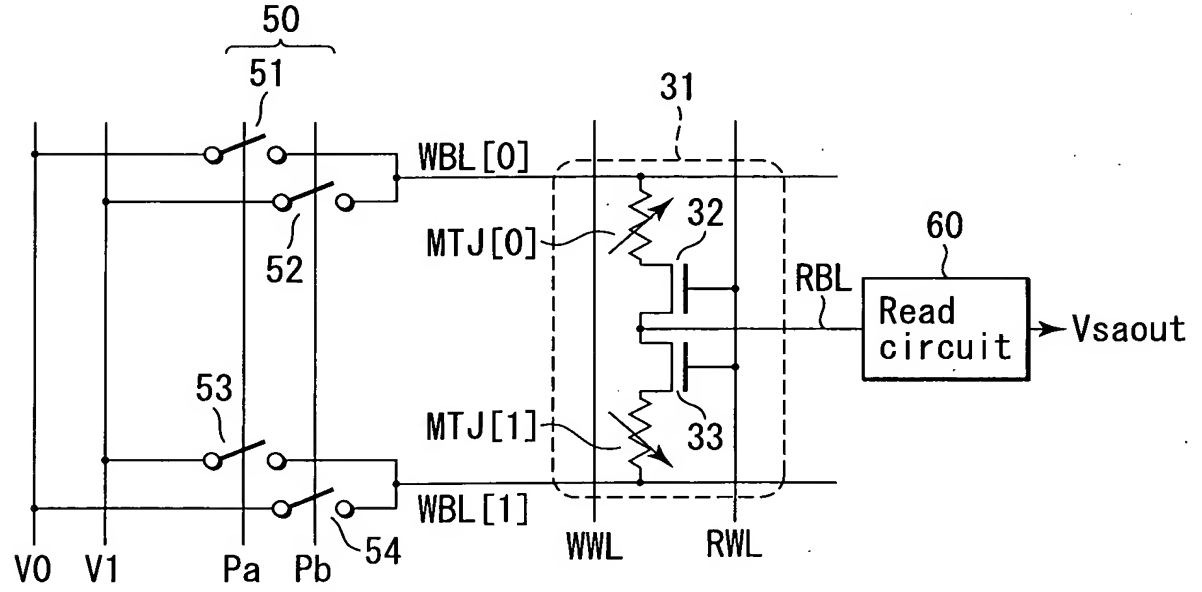

50
51
31
WBL[0]
MTJ[0]
32
60
52
RBL
Read circuit
Vsaout
53
MTJ[1]
33
WBL[1]
V0
V1
Pa
Pb
54
WWL
RWL

FIG. 19

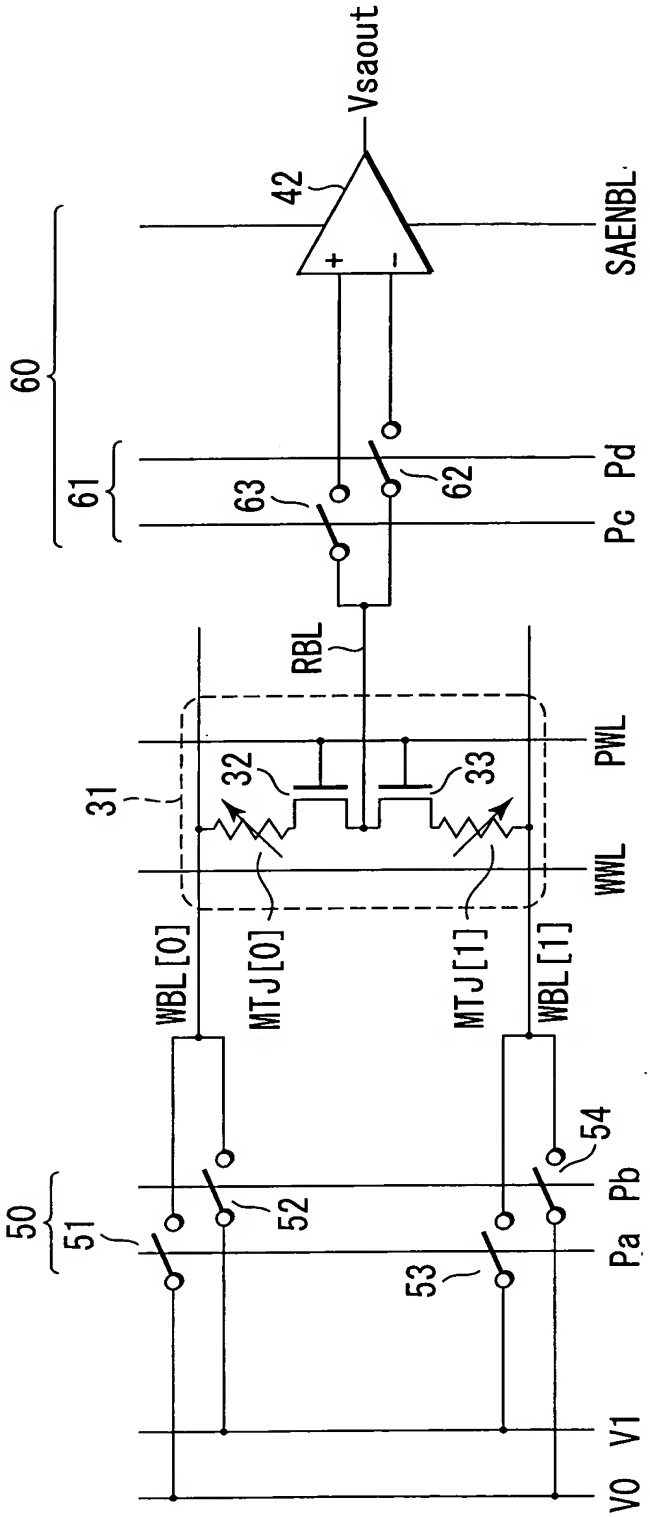

Vsaout
42
SAENBL
60
61
63
62
Pc
Pd
RBL
31
32
33
PWL
WWL
WBL[0]
MTJ[0]
MTJ[1]
WBL[1]
54
50
51
52
53
Pa
Pb
V1
V0

FIG. 20

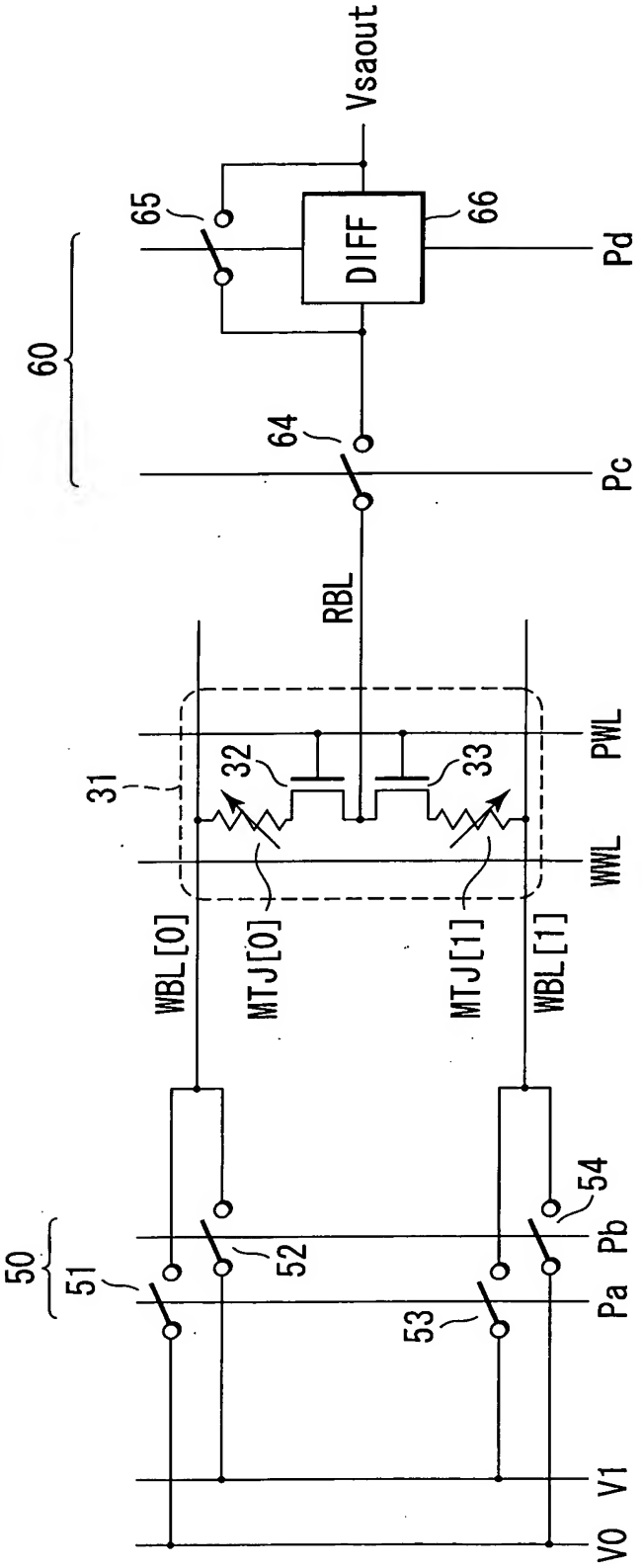

Vsaout
65
DIFF
66
Pd
60
64
Pc
RBL
PWL
32
33
31
WWL
WBL[0]
MTJ[0]
MTJ[1]
WBL[1]
54
50
51
52
Pb
Pa
53
V1
V0

FIG. 21

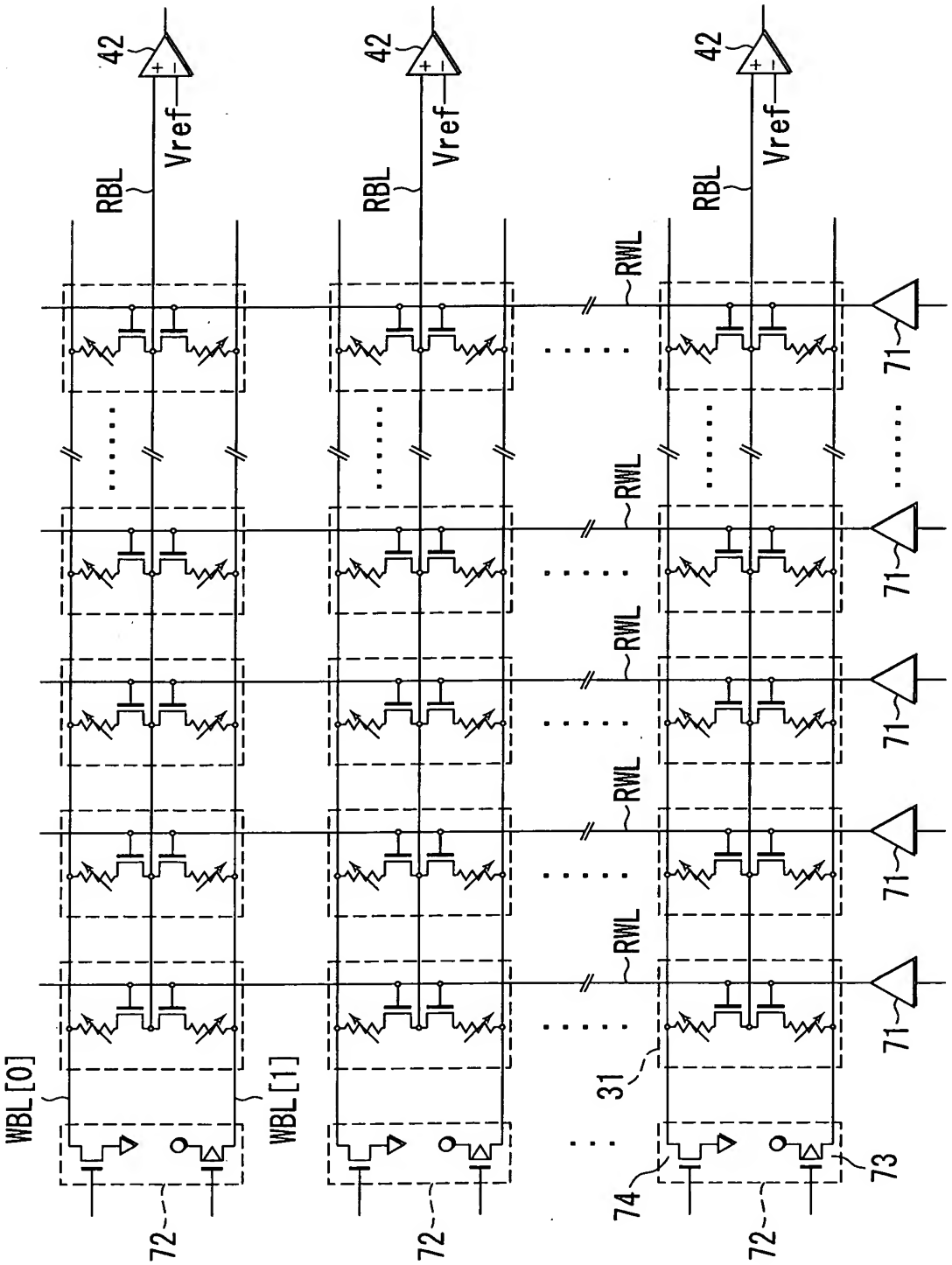


FIG. 22

FIG. 23A

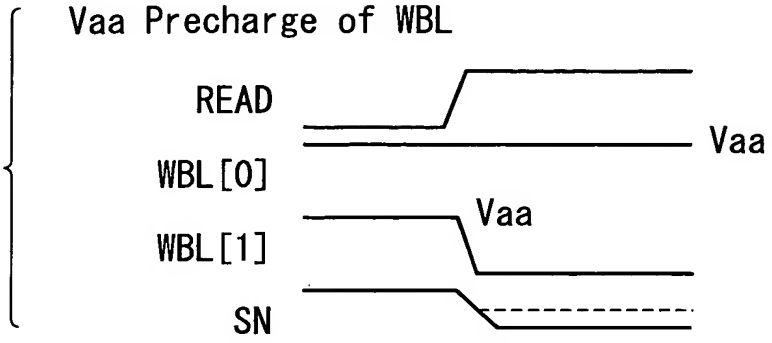


FIG. 23B

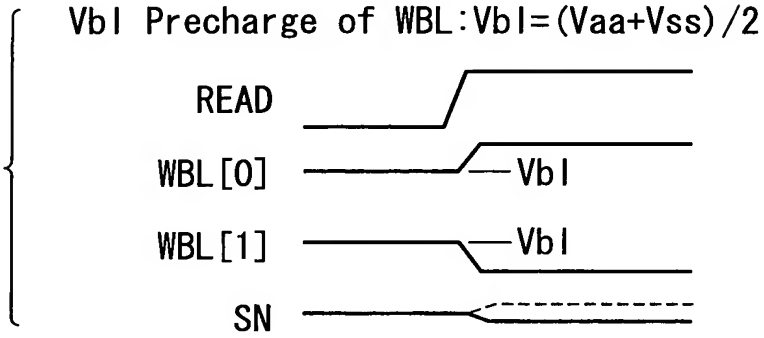


FIG. 23C

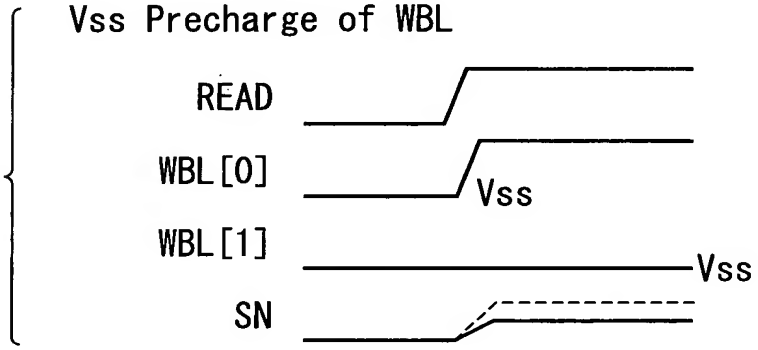


FIG. 24A

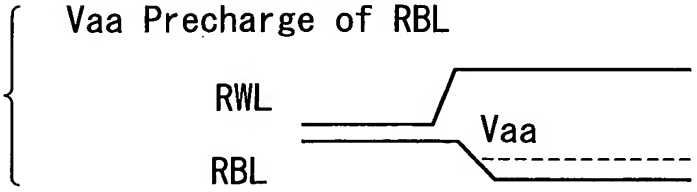


FIG. 24B

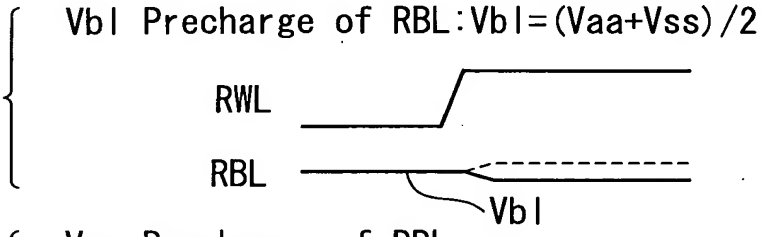
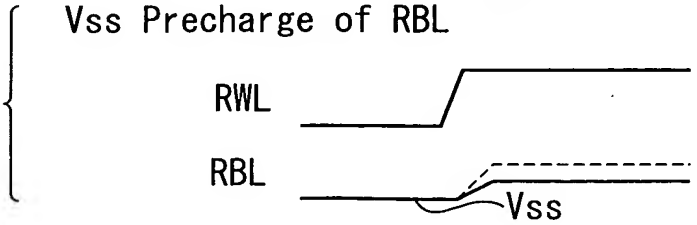


FIG. 24C



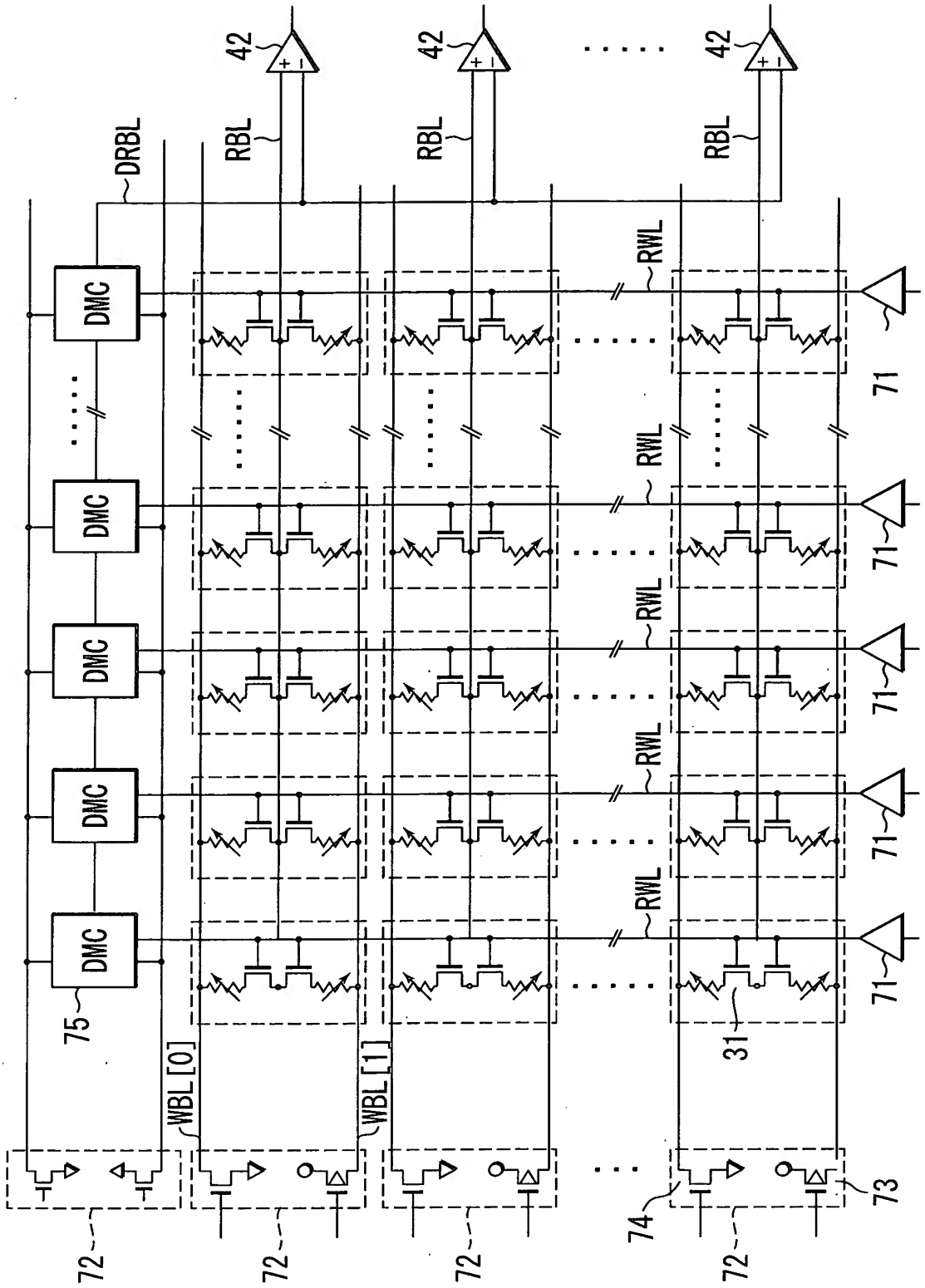


FIG. 25

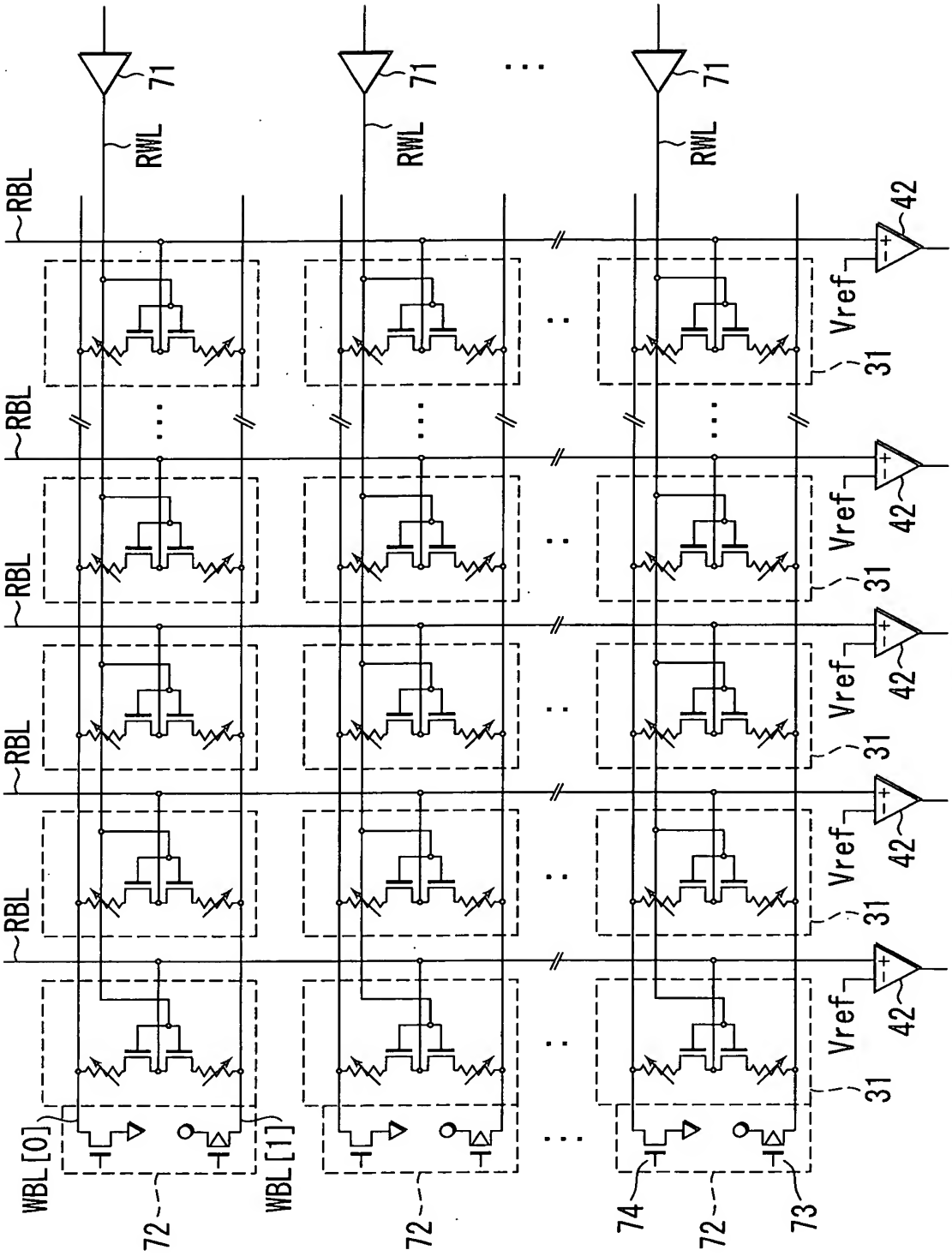


FIG. 26

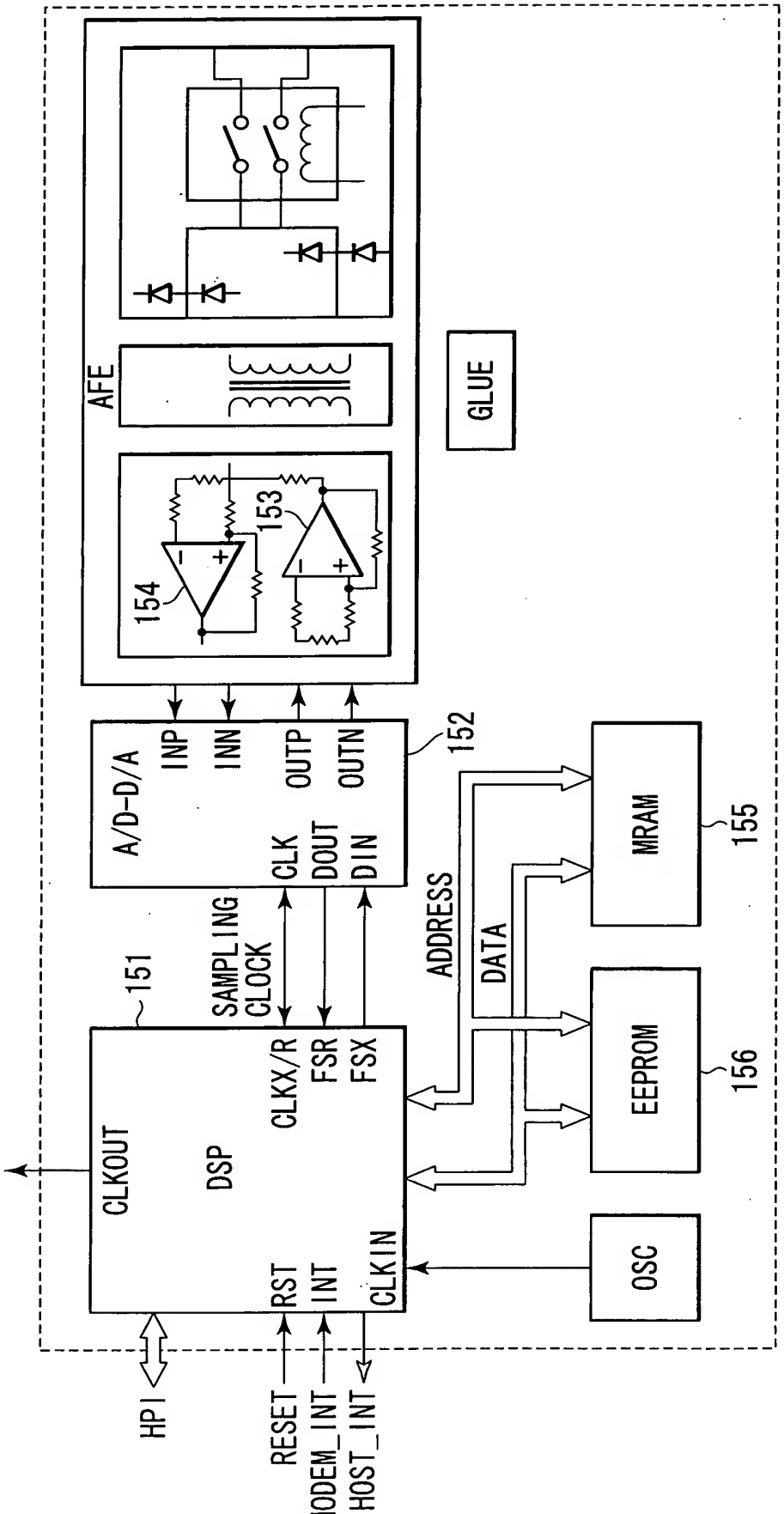

AFE
GLUE
154
153
A/D-D/A
INP
INN
OUTP
OUTN
CLK
DOUT
DIN
152
SAMPLING CLOCK
151
ADDRESS
DATA
MRAM
155
EEPROM
156
CLKOUT
DSP
CLKX/R
FSR
FSX
OSC
RST
INT
CLKIN
HPI
RESET
MODEM_INT
HOST_INT

FIG. 27

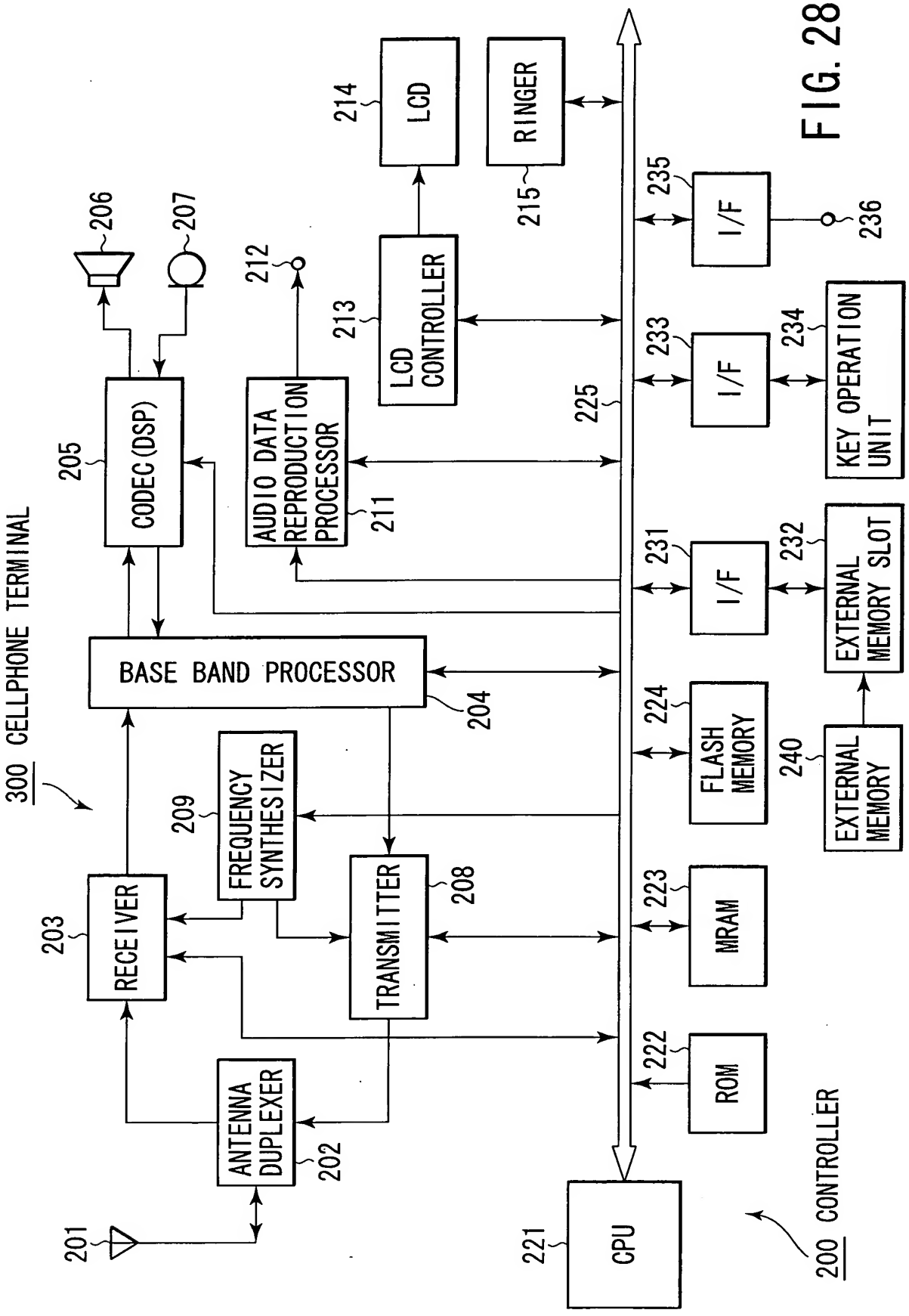

300 CELLPHONE TERMINAL
200 CONTROLLER
201
202
ANTENNA DUPLEXER
203
RECEIVER
204
BASE BAND PROCESSOR
205
CODEC (DSP)
206
207
208
TRANSMITTER
209
FREQUENCY SYNTHESIZER
211
AUDIO DATA REPRODUCTION PROCESSOR
212
213
LCD CONTROLLER
214
LCD
215
RINGER
221
CPU
222
ROM
223
MRAM
224
FLASH MEMORY
225
231
I/F
232
EXTERNAL MEMORY SLOT
233
I/F
234
KEY OPERATION UNIT
235
I/F
236
240
EXTERNAL MEMORY

FIG. 28

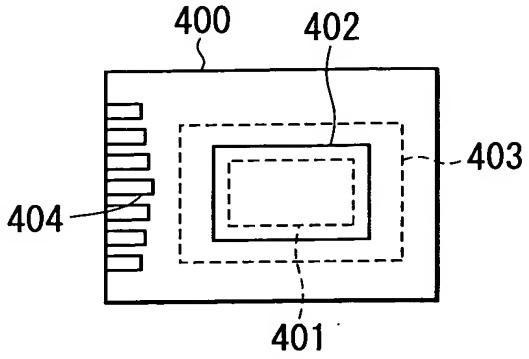


FIG. 29

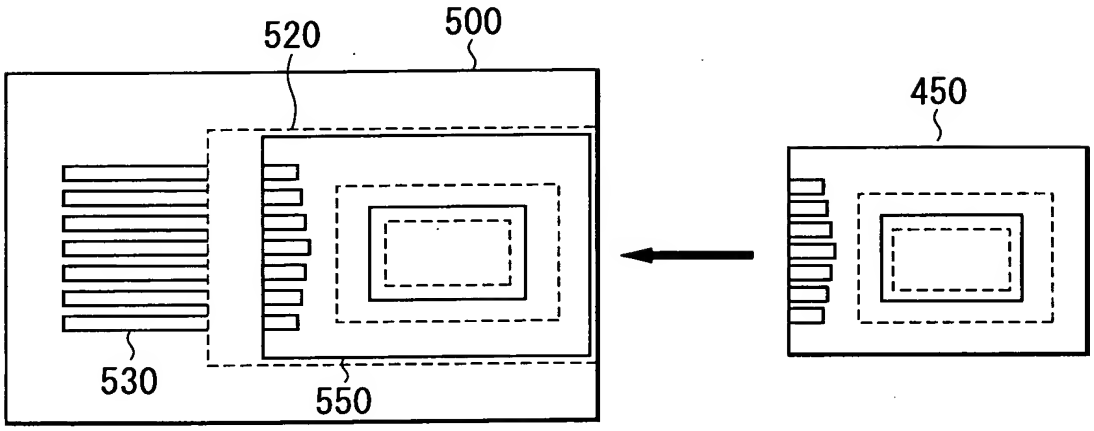
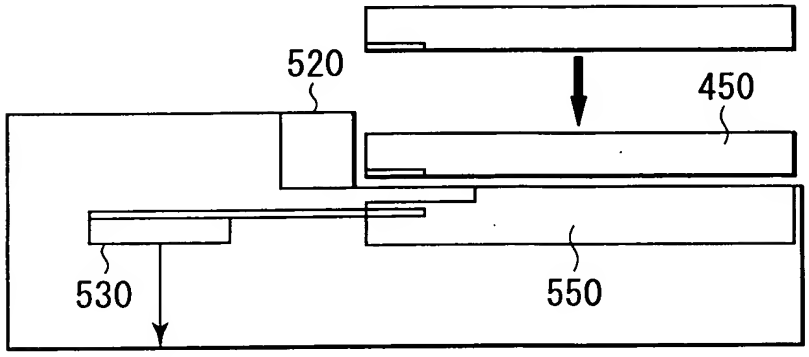


FIG. 30



TO FIRST MRAM DATA REWRITE CONTROLLER

FIG. 32

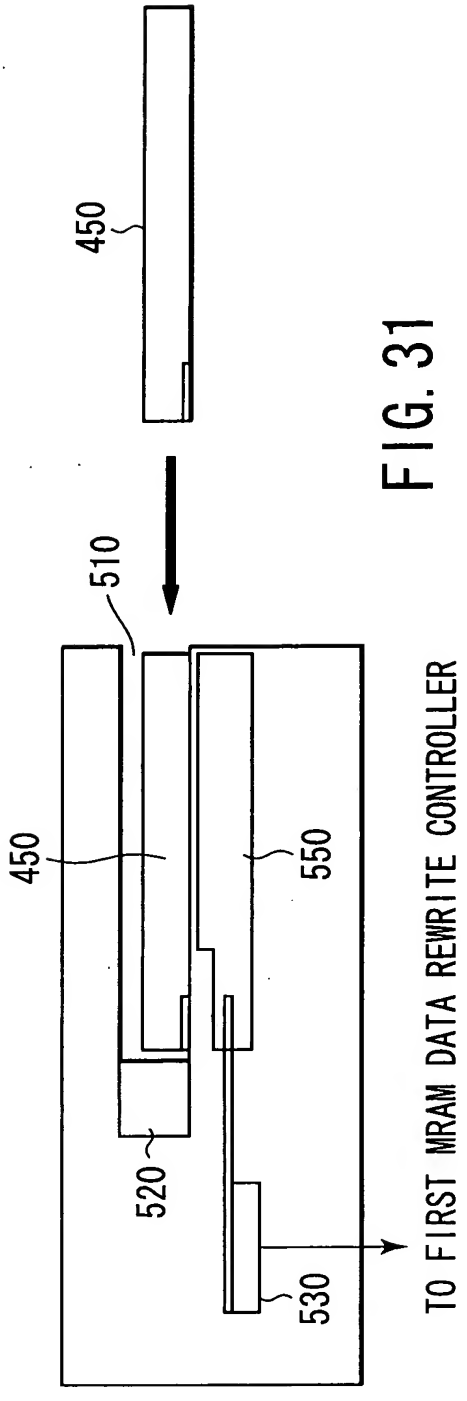

450
510
450
550
520
530
TO FIRST MRAM DATA REWRITE CONTROLLER

FIG. 31

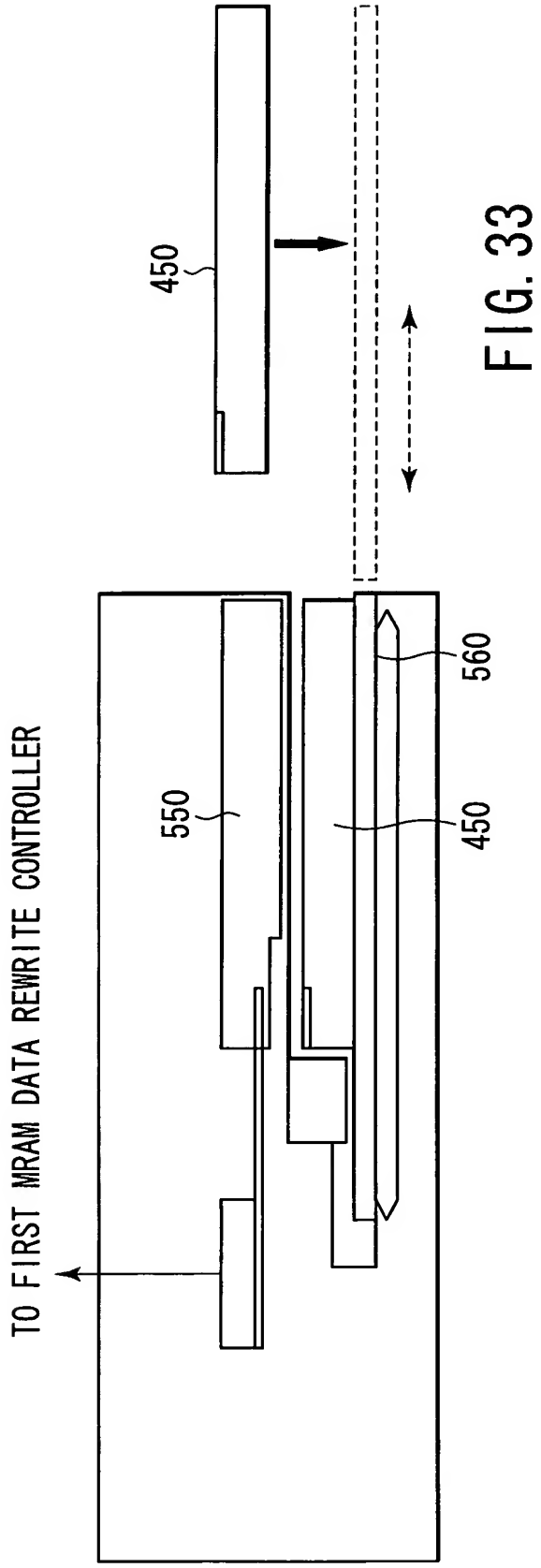

450
560
550
450
TO FIRST MRAM DATA REWRITE CONTROLLER

FIG. 33